Fast Orbit Feedback Control System for the VSX Ring

Masanori SATOH, Kentaro HARADA, Hiroyuki TAKAKI, Tadashi KOSEKI, Norio NAKAMURA and Yukihide KAMIYA
Synchrotron Radiation Laboratory, Institute for Solid State Physics, The University of Tokyo (SRL-ISSP)
3-2-1 Midori-cho, Tanashi, Tokyo 188-8501, Japan
Katsushi HANAWA
TOSHIBA Corp. POWER SYSTEMS & SERVICES COMPANY (FUCHU COMPLEX)
1, Toshiba-cho, Fuchu, Tokyo 183-8511, Japan
Takashi OBINA
Institute of Materials Structure Science, High Energy Accelerator Research Organization (KEK-PF)
1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan

Abstract

A fast orbit feedback system will be installed on the VSX light source being planned at the University of Tokyo [1]. A test feedback control system has been developed. It contains DSP and shared memory boards for fast computation and communication. Although the result of its performance test shows that the processing speed is not perfect for our design goal, it is ascertained that a few improvements in the system can achieve the target performance.

1 Introduction

Orbit stabilization is indispensable to third-generation synchrotron light sources like VSX ring because of their high noise amplification and low beam emittance. A high-performance feedback system should be installed in order to avoid the deterioration of effective photon beam intensity.

A fast feedback control system is required for the VSX ring because the feedback period should be set to 500 μsec to satisfy a desired performance for 128 beam position monitors (BPMs) and 112 steering magnets. A test control system was constructed to check the feasibility of such a fast feedback control. In this paper, we will present the feedback system overview, the test feedback control system and its performance.

2 Feedback System Overview

Figure 1 shows the schematic view of the orbit feedback system we proposed. In our system, four VME units including digital signal processor (DSP) and replicated shared memory boards will be used for feedback control. Since 128 BPMs and 112 steering magnets are installed for measurement and correction of the beam orbit, each VME unit should control 32 BPMs and 28 steering magnets. A DSP board is adopted for high-speed calculations. A shared memory network is used for fast transfer of the BPM data from one VME unit to the others because all BPM data are needed to calculate the excitation currents of the steering magnets.

We already proposed a new COD correction method suitable for orbit feedback, the eigenvector method with constraints [2,3]. This method is also used for usual COD corrections [4]. By the feedback algorithm using this COD correction method, the feedback system can simultaneously perform both functions of the global and local feedbacks in one feedback loop without any interference.

3 Test Feedback Control System

The test system corresponds to one VME unit described in the previous section and consists of a DSP board, an analogue-to-digital converter (ADC) board, a shared memory board, a digital-to-analogue converter (DAC) board, a CPU board and a clock board in a VME crate. The block diagram of the feedback control system and its photograph are shown in figure 2 and 3 respectively. A similar system was already developed [5] and it is successfully operated in the PF ring [6].

The DSP board has two 32-bit floating-point DSPs (Texas Instruments Corp. TMS320C40 [7]), which is 40 MFLOPS (Million Floating point number Operations Per Second) at an instruction cycle of 40MHz. The DSPs perform calculation of the beam positions based on electrode-voltage data of the BPMs, quality check of the position data, calculation of excitation currents of the steering magnets and the PID (proportional, integral and derivative) control. One of them (master DSP) also controls the ADC, DAC and clock boards via a DSP bus.

The shared memory board used in this system is the SCRAMNet board (Sysytran Corp.) with the memory size of 128 kbytes (upgrade memory up to 8 MBytes). The shared memory network achieves real-time communication based on a replicated, shared memory concept. Any memory write to any shared memory board is automatically replicated to all shared memory boards on the network. The data is transferred with about 16 MBytes/s by optical fiber.

The ADC board has 8 channels with 16-bit resolution and it can simultaneously sample and hold all the inputs with a conversion time of 5 μsec. Here, it is assumed that one AD channel treats a BPM with four button electrodes. The test system has only one ADC board, though each VME unit needs 8 ADC board for 32 BPMs. Synchronizing with one trigger signal, each channel digitizes one electrode voltage of each BPM. Therefore, a complete set of the BPM data are obtained after four successive trigger signals.

The DAC board has 8 channels with 16-bit resolution and a conversion time of 13 μsec. It sets the excitation currents to the power supplies of steering magnets. Since each steering magnet provides both horizontal and vertical fields [8], one VME unit needs 7 or 8 DAC boards for 28 steering magnets (56 power supplies).

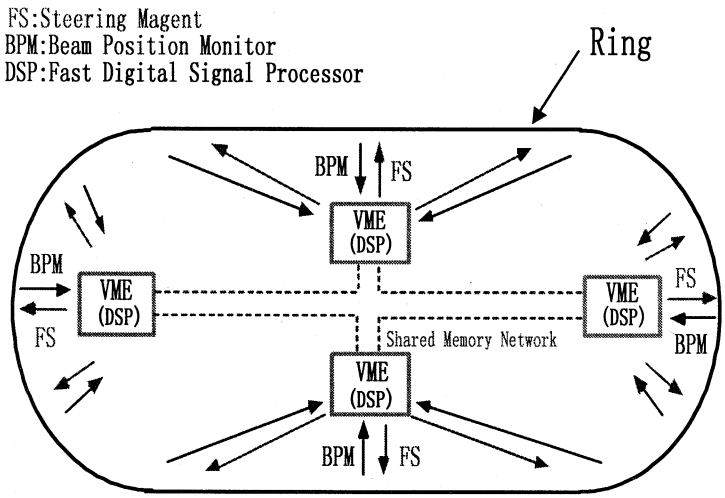

Fig.1 The schematic view of the orbit feedback system

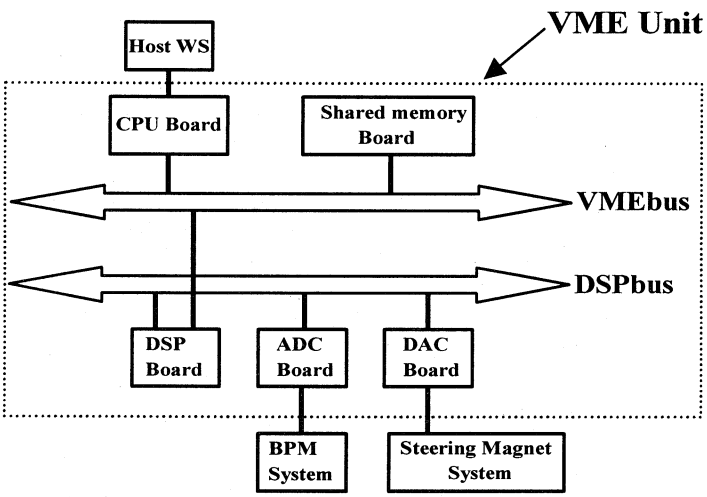

Fig.2 Block diagram of the control system

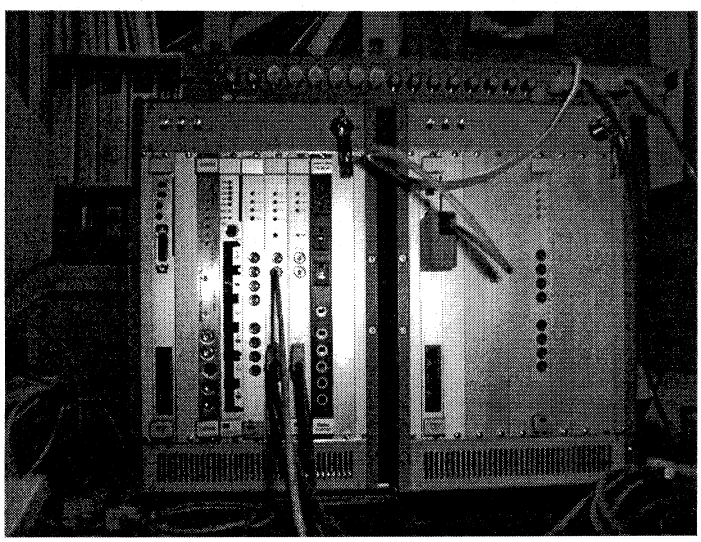

Fig.3 Photograph of the test system for feedback control

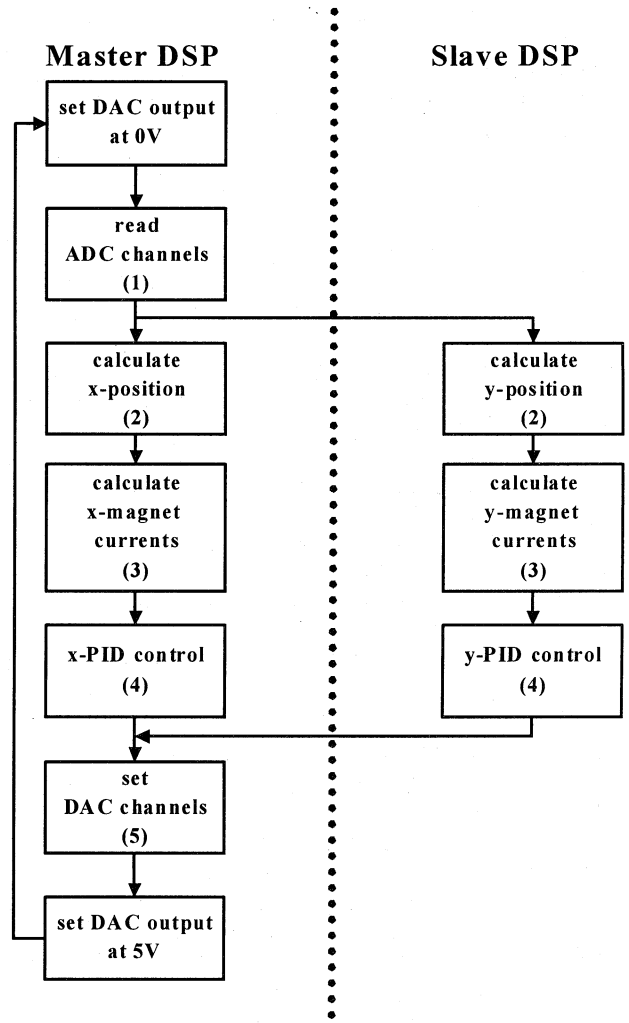

Fig.4 Flowchart of a DSP program simulating the feedback control

Table 1. Result of performance test

Part	Time [μsec]
(1) Read ADC channels	200(150)
(2) Beam position calculation	320(240)
(3) Steering current calculation	420(340)
(4) PID control calculation	80(70)
(5) Set DAC channels	75(75)
Total	1095(875)

*) Time in parentheses means measured time without the shared memory. The excitation current data are written to the shared memory in Part (4).

The CPU board downloads the DSP program from a host workstation to the DSP onboard memory via the Ethernet network port. It also communicates with a database sever in the machine operation. The clock board fixes the feedback period.

4 Performance Test

The performance of the test system was estimated by use of a program which simulates the feedback control. This program contains the following five parts:

(1) Reading four simulated electrode-voltage data of the BPMs from the ADC channels (read ADC channels),
(2) Calculation of the horizontal(x) and vertical(y) beam positions and a quality check of the position data,
(3) Calculation of the horizontal(x) and vertical(y) excitation currents of steering magnets,
(4) Calculation of digital filter outputs for the PID control,
(5) Setting the currents to the DAC channels (set DAC channels).

Figure 4 shows a flowchart of the program. The program was basically coded by C-language for easy modification. However, Parts (3) and (4) were written in assembly language in order to reduce the consumed time. Parallel programming of the two DSPs is used in Parts (2) to (4). The entire program is compiled with a Parallel C compiler [9]. In Parts (1), (2) and (4), the common data are read from and/or written to the shared memory. It includes electrode-voltage, x&y beam-position, x&y current data and several flags. The test was also carried out without the shared memory.

For the performance test, the program forced the master DSP to change the output voltage of a DAC board before and after one computation routine. Therefore, the total computation time was easily measured by an oscilloscope. The consumed time for each part was also measured in the same manner.

Table 1 shows the results of the performance test after optimizing the program. The total time is about 1.1 msec and the majority of it is calculation of the beam positions and steering currents. Access time of shared memory is estimated as about 220 μsec by comparing the total times with and without the shared memory. The data transfer time among the shared memory boards is expected to be about 160 μsec for the shared data of 3 kbytes, though it was not measured in this test. Although Parts (1) and (5) can be reduced when coded in assembly language, its time reduction is only 4 % of the total time.

5 Summary & Future Plan

A fast feedback control system was developed, and its performance was tested. The total time needed for the feedback control was estimated to be about 1.3 msec for the test system, taking account of the data transfer time of the shared memory board.

In the near future, the system performance will be improved by use of a new DSP board, which contains a DSP (Texas Instruments Corp. TMS320C6701) with 1-GFLOPS computational performance at an instruction cycle of 167MHz. Since the C6701 DSP computation power is higher in one order of magnitude than that of two C40 DSPs, the calculation time can be much reduced. In addition, a new shared memory board with the transfer rate of 29.5 Mbytes/s and a DMA controller will be also used to enhance the data transfer and access speed. By these improvements, the desired feedback performance can be attained.

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