TIMING CONTROL FOR TRISTAN

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INTRODUCTION

Outline of the timing control system for TRISTAN is described. This system controls the timing of the devices which operate synchronizing with the magnetic field and the RF frequency of the accumulator ring and the main ring. There are also some devices synchronized with the electron and positron linac.

Since there are many kinds of operation modes for TRISTAN, it must be easy to change the timing control mode from one to another, and to extend the system. And it is also required that the timing signals must be transmitted to many points distributed over the large area of the accelerator sites.

The system includes generation of the timing signals, distribution and reception of them, using the CAMAC system and the transmission system by means of the serial bus of the Manchester II code based on the standard MIL-1553B.[1]

As shown in Fig. 1, since the Manchester II code (bi-phase level code) is transmitted as a bi-polar signal, low susceptibility to noise can be realized due to the use of transformer coupled transmission lines. Then it allows the half-duplex transmission and the transmission of information from numerous sources through one cable. The one word format of the MIL-1553B consists of twenty-bit period with three-bit period for sync, sixteen-bit period for data or command and one bit period for a parity bit. The discrimination of the sync signal polarity distinguishes two kinds of word formats, the command words and the data words. As described later, these words are utilized to transmit the clock signal and the event signals respectively in the timing system.

GLOBAL TIMING SIGNAL

There are three kinds of timing signals for the TRISTAN control which we call "global timing signal". They are:

1. 100 Hz clock signal synchronized with the repetition frequency 50 Hz of the linac.
2. One hundred and twenty-eight event signals coded by seven bits with a dummy identification bit which means the event being in no operation.
3. Time code signal of year, month, day, hour, minute and second.

These signals converted to the Manchester II code are transmitted to CAMAC timing modules on serial multi-drop bus through coaxial cables with the repeater on the way. As shown in Fig. 2, the command sync of the 1553B bus code is used as the clock signal, and the time code data are on the three command words. The event signal is on the data word. The next clock following an event code gives just time of it. We call the clock "event marker". The clock signal has jitter due to the time interval ($\sim$ 1.3 μsec) required in the synchronization between the linac beam and the RF bucket of the accumulator ring, and due to the sampling clock (100 nsec) of the 1553B bus transmission. Order of this jitter is considered to give no problem.

DISTRIBUTION OF THE GLOBAL TIMING SIGNAL AND TIMING MODULES

This system consists of the CAMAC system for the accelerator control linking to the control computer, and the coaxial cables for transmitting the Manchester II code signal of the standard 1553B.

In the central control room there is a CAMAC crate with modules of a master timing generator and a micro-computer for generating and transmitting the global timing signal. CAMAC crates in the local control rooms have timing modules of the repeater and the timing delay (TD1). The repeater recives the global timing signal through the transformer coupled coaxial cable which is terminated with a 50 Ω resister, and retransmits it to the next repeater after shaping the waveform. Simulataneously, it distributes the global timing sig-

nal to the ACL and ACN lines of its own CAMAC dataway and to those of another CAMAC crate which we call "timing bus". When the power supply of the repeater is turned off, the timing signals bypass this module. The time code data can be utilized through the CAMAC dataway and through the connector of the front panel. The timing delay module (TD1) receives the serial Manchester code through the timing bus, separates it into the clock and the required event signal, and converts it to the parallel data using a special integrated circuit (Harris 15530).

The module is preset with the value of delay time from the event signal through the CAMAC dataway. Then it generates the timing pulse used by the control device after counting the number of clock pulses set by the delay from the event signal.

REFERENCE

(1) Computer Design/Dec. 1979 David R. Brickner.

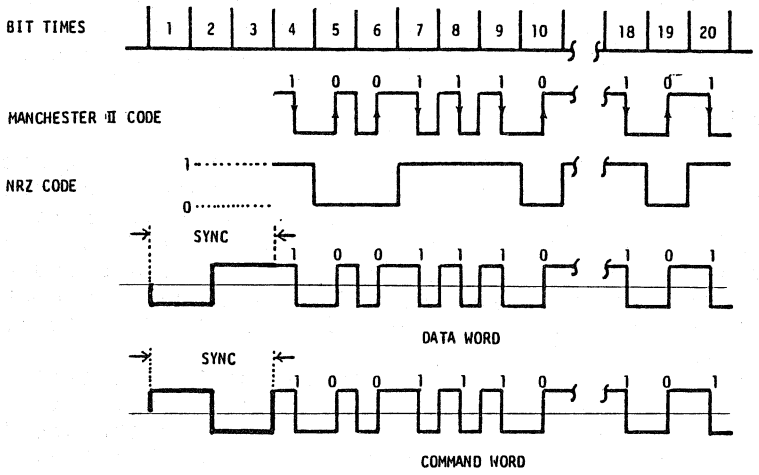

Fig.1 MANCHESTER II CODE AND DATA & COMMAND WORD OF MIL-1553B

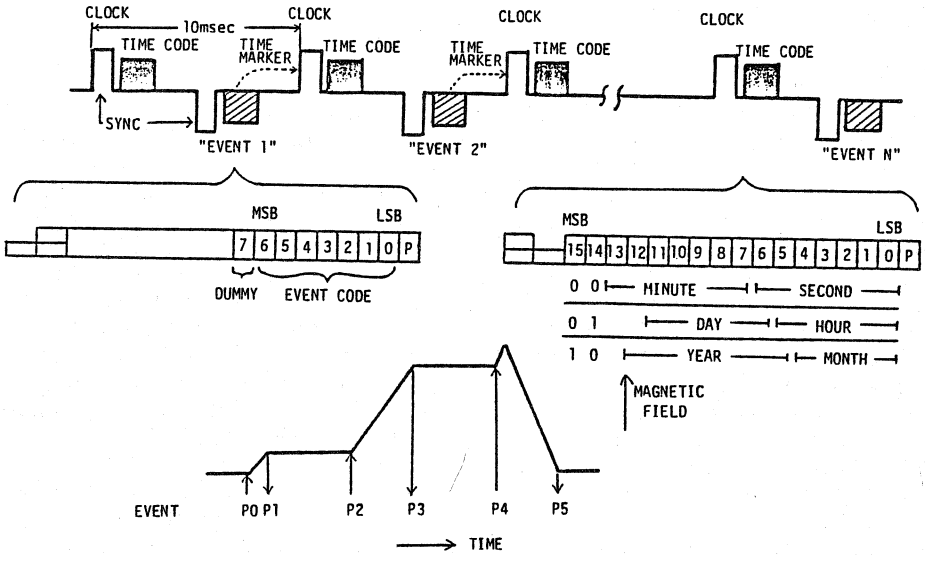

Fig.2 CLOCK,EVENTS AND TIME CODES