PRESENT STATUS OF DIGITAL FEEDBACK AND FEEDFORWARD PROJECT USING RED PITAYA STEMLAB

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Abstract

In all accelerator facilities, a Low-Level RF (LLRF) system is required to stabilize the RF field, to obtain an RF signal with flat amplitude and phase, by suppressing the presence of various disturbances in the RF system. Thus, a new Digital Feedback (DFB) system to be used in the Muon Linac for the muon g-2/EDM Experiment project at J-PARC is built and tested with a simulation test cavity. For that purpose, in our design to build an LLRF setup, the authors have chosen the Red Pitaya STEMlab board featured by high performance, small size, low cost, reconfigurable instrumentation, and open source. J-PARC resources supplied all the needed software and hardware components for the project, such as IQ-Modulator, IQ-Demodulator, and STEMlab board containing Field Programmable Gate Array (FPGA), Analog to Digital Converter (ADC), and Digital to Analog Converter (DAC). The correction of IQ-Modulator and IQ-Demodulator is conducted and the errors are successfully compensated within the control system. The preliminary results of the design and tests of the aforementioned compact DFB system are presented in this paper.

INTRODUCTION

A prototype Red Pitaya DFB system is designed and built to provide a fast and effective LLRF control setup for an accelerator system. The main duty of an LLRF system is to regulate the amplitude and phase of the RF field to compensate disturbances in the RF systems due to variations in temperature and high-voltage power supply (HVPS) ripples etc. The key point of the project is that the Red Pitaya DFB system is built cost-effectively and easy-available to get the all hardware by the use of J-PARC Linac facility resources.

A Red Pitaya STEMlab board [1], a digital electronics platform, with an embedded Linux operating system is used in the system, as a digitizer. An EPICS driver support for the Red Pitaya DFB system is written, based on C programming language and red pitaya-epics [2]. The EPICS IOC is built and tested to control and monitor the Red Pitaya DFB system with a CS-Studio interface. The prototype system has been tested with a test cavity and preliminary results are presented in this paper.

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THE RED PITAYA STEMLAB BOARD

A Red Pitaya board with FPGA Xilinx Zynq 7010 System-On-Chip (SoC) is a hardware module which is used for control instrumentation and laboratory measurement. Red Pitaya is well known for its open-source and also is a cost-efficient data acquisition platform. Moreover, Red Pitaya has 16 single-ended or 8 differential digital I/Os with 3.3V logic levels, one of its digital input is used as an RF GATE in our project. The main reason for choosing Red Pitaya is that Red Pitaya features 2x fast RF inputs on-board which provide a sampling rate of 125Msps each and two output DACs with ±1V voltage range.

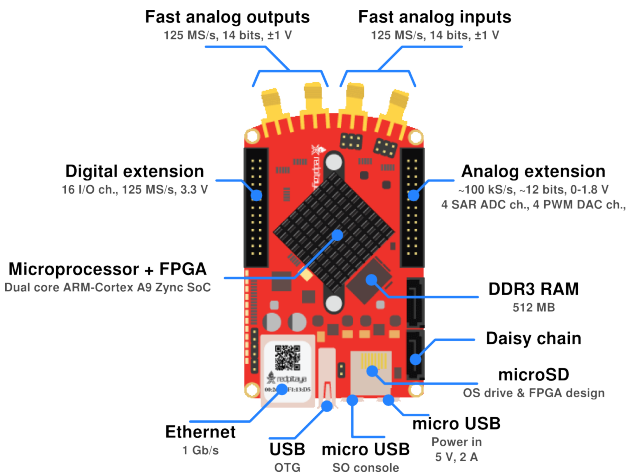

Figure 1: Red Pitaya STEMLab board hardware overview [1].

Fig.1 shows a schematic overview of the Red Pitaya STEMLab125-14 board. The 2x fast ADC input channels have two configurable voltage ranges of ±1 Volt or ±20 Volt. One of the ADC input is for acquiring the In-phase (I) component (ADC1) and the other to acquire the Quadrature (Q) component (ADC2) of the IQ-Demodulator.

PROTOTYPE RED PITAYA DFB PROJECT

The design of the prototype Red Pitaya DFB system is shown in (Fig.2). Adjustable DAC outputs with the Limit module, 2048 samples at 128ns/S, post-mortem use of data for ADC output waveforms to analyze, ADC and DAC rotational functions with correction parameters for IQ-Modulator and Demodulator, a PI (Proportional-Integral) feedback control to obtain a stable RF field for the RF cavity features are provided with the system.

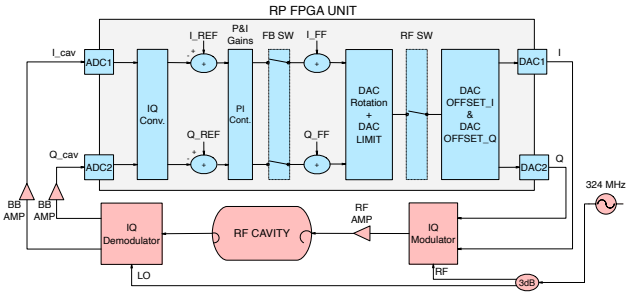

Figure 2: Block diagram of the control system for the Red Pitaya DFB system.

The hardware components used in our project are Red Pitaya STEMlab 125-14 board, an IQ-Modulator, an IQ-Demodulator and an RF amplifier located before the cavity. Also, two baseband (BB) amplifiers that are built at J-PARC by the project team are used to amplify the Demodulator I/Q outputs to be able to use the ADC full scale. The IQ-Demodulator is used after the RF cavity to demodulate the RF cavity signal and convert the amplitude/phase information into I/Q signals which are directed to the ADCs. The IQ-Modulator is used after the DAC outputs of the Red Pitaya DFB system to regenerate an RF signal from I/Q signals which finally drives the RF cavity. 324 MHz signals for RF input of IQ-Modulator and Local Oscillator (LO) of the IQ-Demodulator are generated by Signal Generator.

FPGA Design

FPGA design and construction of the Hardware Description Language (HDL) codes of the Prototype Red Pitaya DFB system are performed by Vivado a Xilinx Software [3]. The very first step is to get the data from ADC1 and ADC2 analog inputs to the FPGA side which is done by ADC core in the ADC-DAC top module. ADC and DAC cores of Red Pitaya are provided in [5] and [6]. Then, ADC outputs are directed to the DFB calculation top module in which all calculations for the DFB system are performed. DAC module is responsible for getting data from the DFB calculation top module and transfer to the DAC analog outputs.

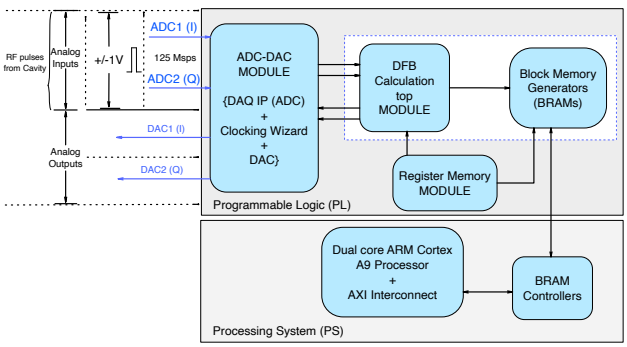

Figure 3: The overview of FPGA block design.

The ZYNQ processing system (PS) communicates with input/output registers provided in the user-created Register Memory module. These registers are used for calculations and monitoring within the DFB top module. PS also communicates with Block Memory Generators (BRAMs) via the Advanced eXtensible Interface (AXI) in the Block Design (Fig.3) provided by Xilinx. These registers contain inputs and outputs needed to update values in EPICS and CS-Studio. Both Registers and BRAMs are accessed with an EPICS driver support written in C programming language. Sign extended ADC outputs go into buffers and are monitored as a waveform.

MEASUREMENTS AND RESULTS

Preliminary tests for the system are conducted on the simulation test cavity. The EPICS Base [4] was cross-compiled and added to the system providing full EPICS server and Channel Access functionality. The EPICS IOC is built and runs on the Red Pitaya Linux operating system to access device driver and supports to create various database records to access Input/Output data such as waveform records to monitor the ADC outputs. Graphical User Interface (GUI) with CS-Studio consisting of three different parts of Main, Monitor, and SET on a remote PC to access the EPICS Process Variables (PVs) is used for monitoring and controlling the whole system. This application provides users to control and monitor system parameters such as IQ conversion, PI control, DAC Rotation with Limit, DAC Offset, and various SET functions.

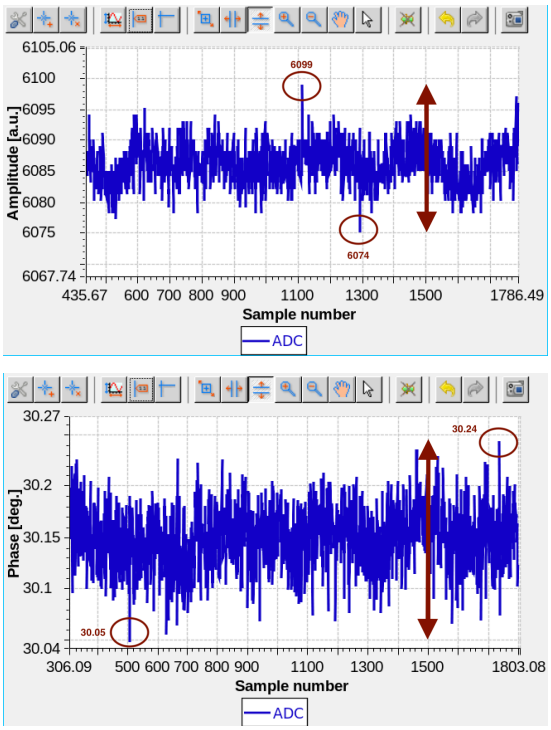

Figure 4: Amplitude and phase stabilities of the RF signal in the cavity. Top: amplitude stability, bottom: phase stability.

Red Pitaya DFB system was tested using "Simulation Cavity" at pulsed operation with an RF signal having a width of 230 μs. The amplitude stability of $\pm$0.21% and phase stability of $\pm$0.10 degrees were evaluated for the RF field of the simulation test cavity without feedback control (Fig.4).

Table 1: Output performance results of the hardware used in the system.

Hardware	Linearity error [%]	Phase error [°]
DAC1	0.32	-
DAC2	0.27	-
ADC1	0.23	<2 (ADC)*
ADC2	0.08	
IQ Mod.	5.4 (**<1**)	-
IQ Demod.	~6 (**0.08**)	~5 (**0.45**)

* Linearity error of the ADC output phase (ADC is the sum of I and Q components).

The performances of hardware used in the Red Pitaya DFB system were investigated. The linearity errors for ADC and DAC I/Q output signals were found to be less than 1%. Also, ADC amplitude and phase calibration was performed and it was found that when linearity between DAC and ADC phase is investigated, there is a significant linear relationship between the variables with an error of less than 2 degrees (Table 1).

IQ-Modulator and Demodulator Errors

The output performances of the IQ-Modulator and Demodulator are also investigated. IQ-Modulator and Demodulator outputs are corrected by Power Meter (PM) and ADCs, respectively. The best performance for the IQ-Modulator is satisfied by the setup which is shown in (Fig.5).

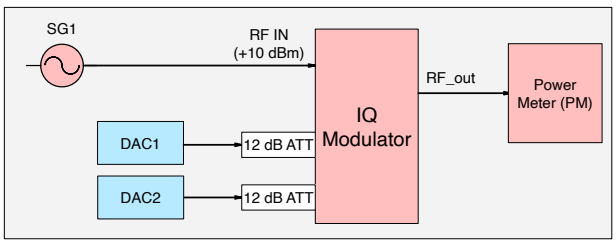

Figure 5: IQ-Modulator power correction setup.

IQ-Modulator RF output is measured by about 220 mV for different DAC outputs with several correction parameter (Δ) (Fig.6). A 12 dB ATT is used before I and Q components to get the best performance, lowest linearity error at the output, in the IQ-Modulator. The linearity error is calculated by about 5.4% for the RF output of the IQ-Modulator without any correction (Δ=0) (Table 1). The error is achieved less than 1% with a correction parameter of 0.045 corresponding to 4.5% variation in amplitude of Q signal (Fig.6). The measurements were performed for a DAC amplitude of 7700 and DAC OFFSET I of -54 and DAC OFFSET Q values of -95 in decimal number.

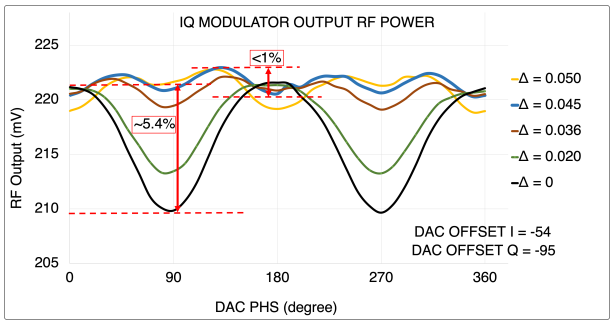

Figure 6: IQ-Modulator power correction results.

The setup to measure the linearity and quadrature-phase balance errors in the IQ-Demodulator is shown in Fig.7. LO input of the IQ-Demodulator is fixed to 10 dBm. RF input power of the Demodulator is fixed to 0.1 dBm. In order to measure linearity error, Demodulator outputs (I and Q signals) are measured at the ADC by sweeping the phase between 0 to 10 V in the phase shifter module. Also, the phase difference between the LO and RF input of the IQ-Demodulator is measured with the Vector Voltmeter (VVM) to measure the phase error of the IQ-Demodulator.

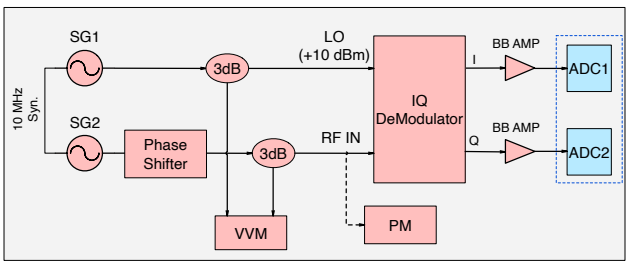

Figure 7: I/Q correction setup for the Demodulator.

The linearity and phase balance errors are measured as 6% and 5 degrees, respectively. These errors are compensated with the correction parameters added to the control system through the EPICS calculations. After the correction, the linearity and phase errors were suppressed to the levels of 0.08% and 0.45 degrees, respectively, which are displayed as bold in Table 1.

CONCLUSION

Hardware and software installation of the prototype Red Pitaya DFB system is carried out. The linearity error of less than 1% is achieved for IQ Modulator output power and a linearity error of 0.08% and phase error of 0.45 degrees for IQ Demodulator output are achieved after correction. The RF field in the simulation test cavity is measured within $\pm$1 degrees in phase and $\pm$1% in amplitude has been successfully met. The setup can be operated in pulsed mode in RF cavity systems and is highly effective for the RF pulses up to 230 μs. Hence, the Red Pitaya DFB system will be used in the Linac section dedicated to the Muon acceleration for Muon

g-2/EDM Experiment project at J-PARC, under the condition that the cavities are operated with short RF pulses [7]. Also, the setup can be used in an RFQ cavity [8] in which the accelerator system is operating in pulsed mode with 100 μs RF pulse length.

The total cost of the project is about 70k JPY which is one of the key points of our system. Furthermore, since IQ-Modulator and Demodulator are the passive RF components, the system will be upgraded with higher performance and less error bearing components. However, the errors for these components are compensated by calculations within EPICS (I/Q correction) in our setup. Moreover, P gain is already satisfied in the PI-feedback control and the study for I gain will be performed as a next step. As a result, it is also planned to upgrade the system to operate for 500 μs RF pulses. Then, PI Feedback control will be tested in R&D of RFQ IV which has been installed in Test Stand (TS) and Klystron TS in J-PARC.

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REFERENCES

[1] "Red Pitaya STEMlab 125-14'
`https://www.redpitaya.com`

[2] "redpitaya-epics'
`https://github.com/AustralianSynchrotron/redpitaya-epics`

[3] "Vivado Design Suite HLx Editions - Accelerating High Level Design'
`https://www.xilinx.com/products/design-tools/vivado.html`

[4] "EPICS Base, Experimental Physics and Industrial Control System"
`https://epics.anl.gov/base/index.php`

[5] "Koheron SDK"
`https://github.com/Koheron/koheron-sdk/tree/master/examples/red-pitaya`

[6] "red-pitaya-notes"
`https://github.com/pavel-demin/red-pitaya-notes`

[7] Nakazawa, Y., "Beam commissioning of muon beamline using negative hydrogen ionsgenerated by ultraviolet light" Nuclear Inst. and Methods in Physics Research, A, 937 (2019) 164–167.

[8] Cicek, E., "Electromagnetic simulations, manufacturing and low power measurements of a 352.21 MHz RF power coupler for the SANAEM RFQ project" Journal of Instrumentation, 13, T10005, 2018.